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September 6, 2006

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Art Unit 2183

Attn: Mail Stop Appeal Brief - Patents

Re: U.S. Utility Patent Application
Application No. 09/395,294; Filed: September 13, 1999
For: **An Instruction Set For A Computer**
Inventor: Sophie WILSON
Our Ref: 1875.5790000

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Copy of the Notification of Non-Compliant Appeal Brief;

2. Brief on Appeal Under 37 C.F.R. §41.37, including Exhibits A, B and C thereto (one copy); and

3. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

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BSW/smn
Enclosures

579605_1.DOC

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/395,294	09/13/1999	SOPHIE WILSON	1073/OG117	5796

26111 7590 08/09/2006

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EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Appeal Brief due September 9, 2006

Notification of Non-Compliant Appeal Brief (37 CFR 41.37)	Application No. 09/395,294	Applicant(s) WILSON, SOPHIE
	Examiner Tonia L. Meonske	Art Unit 2181

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

The Appeal Brief filed on *08 September 2005* is defective for failure to comply with one or more provisions of 37 CFR 41.37.

To avoid dismissal of the appeal, applicant must file anamended brief or other appropriate correction (see MPEP 1205.03) within **ONE MONTH or THIRTY DAYS** from the mailing date of this Notification, whichever is longer. **EXTENSIONS OF THIS TIME PERIOD MAY BE GRANTED UNDER 37 CFR 1.136.**

1. ☐ The brief does not contain the items required under 37 CFR 41.37(c), or the items are not under the proper heading or in the proper order.

2. ☐ The brief does not contain a statement of the status of all claims, (e.g., rejected, allowed, withdrawn, objected to, canceled), or does not identify the appealed claims (37 CFR 41.37(c)(1)(iii)).

3. ☐ At least one amendment has been filed subsequent to the final rejection, and the brief does not contain a statement of the status of each such amendment (37 CFR 41.37(c)(1)(iv)).

4. ☒ (a) The brief does not contain a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number and to the drawings, if any, by reference characters; and/or (b) the brief fails to: (1) identify, for each independent claim involved in the appeal and for each dependent claim argued separately, every means plus function and step plus function under 35 U.S.C. 112, sixth paragraph, and/or (2) set forth the structure, material, or acts described in the specification as corresponding to each claimed function with reference to the specification by page and line number, and to the drawings, if any, by reference characters (37 CFR 41.37(c)(1)(v)).

5. ☐ The brief does not contain a concise statement of each ground of rejection presented for review (37 CFR 41.37(c)(1)(vi))

6. ☐ The brief does not present an argument under a separate heading for each ground of rejection on appeal (37 CFR 41.37(c)(1)(vii)).

7. ☐ The brief does not contain a correct copy of the appealed claims as an appendix thereto (37 CFR 41.37(c)(1)(viii)).

8. ☐ The brief does not contain copies of the evidence submitted under 37 CFR 1.130, 1.131, or 1.132 or of any other evidence entered by the examiner **and relied upon by appellant in the appeal**, along with a statement setting forth where in the record that evidence was entered by the examiner, as an appendix thereto (37 CFR 41.37(c)(1)(ix)).

9. ☐ The brief does not contain copies of the decisions rendered by a court or the Board in the proceeding identified in the Related Appeals and Interferences section of the brief as an appendix thereto (37 CFR 41.37(c)(1)(x)).

10. ☒ Other (including any explanation in support of the above items):

In support of item 4(a) above, the brief does not contain a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, including a correspondence of each claimed function with reference to the specification by page, line number and drawing reference characters. The summary of claimed subject matter section fails to specifically mention any of the independent claims involved in the appeal, such as claims 17, 24, 28, 32 and 33. All of the independent claims are different, such that they would have different claim summaries. The summary of claimed subject matter section should countain a concise explanation of each independent claim involved in the appeal, specifially of claims 17, 24, 28, 32 and 33. Appropriate correction is required.

TONIA L. MEONSKE

Tonia L. Meonske 08/04/2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Sophie Wilson
Appl. No.: 09/395,294
Filed: September 13, 1999
For: **An Instruction Set for a Computer**

Confirmation No. 5796
Art Unit: 2183
Examiner: T. Meonske
Atty. Docket: 1875.5790000

Brief On Appeal Under 37 C.F.R. § 41.37

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Notice of Appeal from the final rejection of claims 17-33 for the above-captioned U.S. patent application was filed on January 19, 2005, together with the required fee of $500 under 37 C.F.R. § 41.20(b)(1) for a large entity. A Brief on Appeal under C.F.R. § 41.37 was filed by Appellant on May 17, 2005. A Notification of Non-Compliant Appeal Brief was mailed on August 9, 2005. In response to the Notification of Non-Compliant Appeal Brief, a revised Brief on Appeal under C.F.R. § 41.37 was filed by Appellant on September 9, 2005. A second Notification of Non-Compliant Appeal Brief was mailed on August 9, 2006. In response to the second Notification of Non-Compliant Appeal Brief, Appellant hereby files this Brief on Appeal Under 37 C.F.R. § 41.37. The required brief filing fee of $500.00 under 37 C.F.R. § 41.20(b)(2) for a large entity was submitted with Appellant's filing on May 17, 2005.

The Commissioner is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Table of Contents

I. Real Party in Interest (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is Broadcom Corporation, having its principal place of business at 16215 Alton Parkway, Irvine, California 92618. An assignment assigning all right, title and interest in and to the above-captioned patent application from inventor Sophie Wilson to Broadcom Corporation was recorded in the U.S. Patent & Trademark Office (USPTO) on June 9, 2000 at Reel 010873, Frame 0652.

II. Related Appeals and Interferences (37 C.F.R. § 41.37(c)(1)(ii))

Appellant, including the undersigned legal representative and the assignee of the above-captioned application, are aware of no pending appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board of Patent Appeals and Interferences ("the Board") in the pending appeal.

III. Status of the Claims (37 C.F.R. § 41.37(c)(1)(iii))

This application was filed on September 13, 1999 and assigned U.S. Application No. 09/395,294 ("the '294 application"). The '294 application included claims 1-16. In an Amendment and Response to Office Action filed April 15, 2002, claim 13 was cancelled, and claims 12 and 14 were amended. In an Amendment and Response to Office Action filed December 20, 2002, claims 3, 12, and 15 were amended. In an Amendment and Response to Office Action filed July 3, 2003, claims 2 and 3 were cancelled, and claims 1, 12, and 14-16 were amended. In an Amendment and Reply Under 37 C.F.R. § 1.116 filed March 24, 2004, claims 1, 4-12,

and 14-16 were cancelled, and new claims 17-33 were added. As such, claims 17-33 are currently pending in the present application.

In an Amendment and Reply Under 37 C.F.R. § 1.111 filed July 16, 2004, claims 17, 24, 28, 32, and 33 were amended

A Final Rejection rejecting claims 17-33 was mailed on October 19, 2004 (the "Final Rejection"). The Final Rejection incorporated by reference the several grounds of rejection set forth in the Office Action mailed April 16, 2004 (the "Office Action"). A Notice of Appeal was filed on January 19, 2005. Claims 17-33 are on appeal. A copy of the claims on appeal can be found in the attached Claims Appendix.

IV. Status of Amendments (37 C.F.R. § 41.37(c)(1)(iv))

No amendments have been filed by Appellant subsequent to the Examiner's Final Rejection.

V. Summary of the Claimed Subject Matter (37 C.F.R. § 41.37(c)(1)(v))

The present invention is directed to an instruction set for a computer.

Overview

A very long instruction word (VLIW) is a type of instruction set that includes multiple instructions that may be executed simultaneously. (Specification, p. 1, line 21). Each instruction of the VLIW has the same bit length, meaning that each instruction includes the same number of bits. (Specification, p. 1, lines 21-22). The

VLIW has a first bit length, and each instruction of the VLIW has a second bit length. (Specification, p. 1, lines 21-22; p. 5, lines 14-16; FIG. 5, elements L1, L2, and L3).

The VLIW arrangement avoids misalignment problems associated with some other types of instruction set arrangements, which allow instructions to be of different lengths. However, the length of each instruction of the VLIW, and therefore the potential complexity of respective instructions, is limited.

The present invention solves this problem by allowing an instruction of the VLIW to define a single operation or multiple independent operations. (Specification, p. 6, line 28 - p. 7, line 9; p. 7, lines 25-32; FIGs. 2a and 2b).

An instruction of a VLIW can be a long instruction defining a single operation (FIG. 2b), or a dual operation instruction defining two independent operations (FIG. 2a). (Specification, p. 5, lines 14-17; p. 6, line 28 - p. 7, line 9; p. 9, lines 27-28). Each instruction of the VLIW may include identification bits at designated bit locations in the instruction. (Specification, p. 6, line 31 - p. 7, line 9; FIGs. 2a and 2b, elements ID1 and ID2). The identification bits have a dual purpose: denoting whether the instruction is a long instruction or a dual operation instruction and identifying the type of operations in a dual operation instruction. (Specification, p. 6, line 31 - p. 7, line 9).

Independent claim 17

Independent claim 17 recites a system to process VLIWs, the system comprising: a decode unit to decode an instruction of a VLIW received during an instruction fetch (Specification, p. 5, lines 14-16; FIG. 1, element 4), wherein all instructions of the VLIW have the same predetermined instruction bit length

(Specification, p. 1, lines 20-28; p. 5, lines 14-17; FIG. 5, elements L1, L2, and L3), and first and second processing channels (Specification p. 5, lines 17-20; FIG. 1, elements 5x and 5y), each processing channel including a plurality of functional units (Specification, p. 5, lines 19-20; FIG. 1, elements MAC_x, INT_x, FPU_x, LSU_x, MAC_y, INT_y, FPU_y, and LSU_y), at least one of the functional units of each processing channel being a data processing unit (Specification p. 5, lines 19-20; FIG. 1, elements MAC_x, INT_x, FPU_x, MAC_y, INT_y, and FPU_y) and at least one other of the functional units of each processing channel being a memory access unit (Specification p. 5, lines 19-20; FIG. 1, elements LSU_x and LSU_y), wherein the decode unit is operable to determine whether the instruction defines a single operation or two independent operations and to control the first and second processing channels based on the determination (Specification, p. 5, lines 14-17; p. 6, lines 29-31; p. 7, lines 8-9; p. 9, line 24 - p. 10, line 22; FIG. 1, elements 5_x and 5_y; FIGs. 2a and 2b).

Independent claim 24

Independent claim 24 recites a method of operating a system that processes very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length (Specification, p. 1, lines 20-28; p. 5, lines 14-17; FIG. 5, elements L1, L2, and L3), the method comprising: decoding an instruction of the VLIW received during an instruction fetch to determine whether the instruction defines a single operation or two independent operations (Specification, p. 5, lines 14-17; p. 6, lines 29-31; p. 7, lines 8-9; p. 9, line 24 - p. 10, line 22; FIGs. 2a and 2b), when the instruction defines two independent operations, supplying one of the independent operations to a first processing channel having a first plurality of

functional units including a first data processing unit and a first memory access unit (Specification, p. 5, lines 17-20; p. 9, line 24 - p. 10, line 3; FIG. 1, elements MAC_x, INT_x, FPU_x, LSU_x, MAC_y, INT_y, FPU_y, and LSU_y), and supplying the other of the independent operations to a second processing channel having a second plurality of functional units including a second data processing unit and a second memory access unit (Specification, p. 5, lines 17-20; p. 9, line 24 - p. 10, line 3; FIG. 1, elements MAC_x, INT_x, FPU_x, LSU_x, MAC_y, INT_y, FPU_y, and LSU_y), wherein the two independent operations are executed simultaneously (Specification, p. 7, lines 18-19; p. 10, lines 3-5), and when the instruction defines a single operation, controlling the first and second processing channels to cooperate to execute the single operation (Specification, p. 10, lines 7-22).

Independent claim 28

Independent claim 28 recites an article comprising a medium for storing commands (Specification, p. 5, lines 10-12) to enable a processor-based system to: process very long instruction word data including very long instruction words (VLIWs) (Specification, p. 1, lines 20-22; p. 6, lines 28-29), each instruction of a VLIW having the same predetermined instruction bit length (Specification, p. 1, lines 20-28; p. 5, lines 14-17; FIG. 5, elements L1, L2, and L3), wherein the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch to determine whether the instruction defines a single operation or two independent operations (Specification, p. 5, lines 14-17; p. 6, lines 29-31; p. 7, lines 8-9; p. 9, line 24 - p. 10, line 22; FIGs. 2a and 2b),

when the instruction defines two independent operations, supply one of the independent operations to a first processing channel and supply the other of the independent operations to a second processing channel (Specification, p. 5, lines 17-20; p. 9, line 24 - p. 10, line 3; FIG. 1, elements 5_x and 5_y), wherein the two independent operations are executed simultaneously (Specification, p. 7, lines 18-19; p. 10, lines 3-5), and when the instruction defines a single operation, control the first and second processing channels to cooperate to execute the single operation (Specification, p. 10, lines 7-22; FIG. 1, elements 5_x and 5_y).

Independent claim 32

Independent claim 32 recites a method of operating a system that processes very long instruction words (VLIWs) (Specification, p. 1, lines 20-22; FIG. 1), each instruction of a VLIW having the same predetermined instruction bit length (Specification, p. 1, lines 20-28; p. 5, lines 14-17; FIG. 5, elements L1, L2, and L3) and at least one identification bit at at least one predetermined bit location in the instruction (Specification, p. 6, line 31 - p. 7, line 32; p. 8, lines 4-6; FIGs. 2a and 2b, elements ID1 and ID2; FIGs. 3 and 4, elements M (bit 31) and G (bits 29 and 30); FIG. 5, bits 63 and 29-31), the method comprising: fetching the VLIW from a program memory (Specification, p. 5, lines 14-16; p. 9, lines 25-26; FIG. 1, element 2), decoding each instruction of the VLIW (Specification, p. 5, lines 17-19; p. 9, lines 27-28), wherein decoding each instruction includes reading the identification bit of each instruction (Specification, p. 9, lines 27-28) to determine: a) whether the instruction defines a single operation or two independent operations (Specification, p. 5, lines 14-17; p. 6, line 28 - p. 7, line 13; p. 9, line 27 - p. 10, line 22; FIGs. 2a and

2b), and b) when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation (Specification, p. 7, lines 15-32; p. 9, line 28 - p. 10, line 3).

Independent claim 33

Independent claim 33 recites an article comprising a medium for storing commands (Specification, p. 5, lines 10-12) to enable a processor-based system to: process very long instruction word data including very long instruction words (VLIWs) (Specification, p. 1, lines 20-22; p. 6, lines 28-29), each instruction of a VLIW having the same predetermined instruction bit length (Specification, p. 1, lines 20-28; p. 5, lines 14-17; FIG. 5, elements L1, L2, and L3) and at least one identification bit at at least one predetermined bit location in the instruction (Specification, p. 6, line 31 - p. 7, line 32; p. 8, lines 4-6; FIGs. 2a and 2b, elements ID1 and ID2; FIGs. 3 and 4, elements M (bit 31) and G (bits 29 and 30); FIG. 5, bits 63 and 29-31), wherein the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch (Specification, p. 5, lines 14-19; p. 9, lines 25-28) to determine: a) whether the instruction defines a single operation or two independent operations (Specification, p. 5, lines 14-17; p. 6, line 28 - p. 7, line 13; p. 9, line 27 - p. 10, line 22; FIGs. 2a and 2b), and b) when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data

processing category of operation and a memory access category of operation (Specification, p. 7, lines 15-32; p. 9, line 28 - p. 10, line 3).

VI. Grounds of Rejection to be Reviewed (37 C.F.R. § 41.37(c)(1)(vi))

The grounds of rejection to be reviewed on appeal are:

A. whether claims 17-20, 24, and 25 are patentable under 35 U.S.C. § 102(b) over U.S. Patent No. 6,317,820 to Shiell et al. ("Shiell"), attached hereto as Exhibit A;

B. whether claims 21-23, 26, 27, and 32 are patentable under 35 U.S.C. § 103(a) over Shiell in view of U.S. Patent No. 5,761,470 to Yoshida ("Yoshida"), attached hereto as Exhibit B;

C. whether claim 28 is patentable under 35 U.S.C. § 103(a) over Shiell in view of U.S. Patent No. 6,697,774 to Panesar ("Panesar"), attached hereto as Exhibit C; and

D. whether claims 29-31 and 33 are patentable under 35 U.S.C. § 103(a) over Shiell in view of Yoshida and Panesar.

A copy of each of the aforementioned documents is attached for the Board's convenience.

VII. Argument (37 C.F.R. § 41.37(c)(1)(vii))

In the remarks that follow, the rejection of each claim is separately discussed. Appellant recognizes that any claim that depends from a patentable independent claim

is patentable at least by virtue of its dependency. In addition, claims 18-23, which depend from claim 17, claims 25-27, which depend from claim 24, and claims 29-31, which depend from claim 28, are patentable not only in view of their dependencies, but also by virtue of their specifically recited features.

There are four separate grounds of rejection to be reviewed on appeal.

A. The rejection of claims 17-20, 24, and 25 under 35 U.S.C. § 102(b) as being allegedly anticipated by Shiell is improper and must be reversed

In section 2 of the final Office Action, the Examiner rejected claims 17-20, 24, and 25 under 35 U.S.C. § 102(b) as being allegedly anticipated by Shiell. Appellant respectfully traverses this rejection. The patentability of each of claims 17-20, 24, and 25 is separately discussed below.

Claim 17

Claim 17 recites, among other features,

> a decode unit to decode ***an instruction of a VLIW*** received during an instruction fetch, ... wherein the decode unit is operable to determine whether ***the instruction defines a single operation or two independent operations*** and to control the first and second processing channels based on the determination.

VLIW is an abbreviation for "very long instruction word", which is a term of art. A VLIW is a type of instruction set that includes multiple instructions, which may be executed in parallel on different functional units of a processor. Claim 17 calls for a decode unit that is operable to determine whether an instruction of a VLIW defines a single operation or two independent operations.

In the Final Rejection, the Examiner stated:

> Shiell et al. have in fact taught an instruction of a VLIW (abstract, column 3, lines 50-67, The processor is a VLIW that processes VLIW instructions.) received during an instruction fetch (column 4, lines 1-5) can define a single operation or two independent operations (column 2, lines 52-56, The VLIW instructions can change the processor from the first mode (the execution of a single operation), or the second mode (the execution of two independent operations)).

Final Rejection, dated October 19, 2004, at p. 3.

Appellant respectfully submits that the Examiner has misunderstood Shiell's teachings. The system in Shiell is described with respect to a Texas Instruments TMS320C62x/C67x ("C6x") family of processors. Shiell describes a C6x processor, as illustrated in FIG. 1 of Shiell, as follows:

> [T]his type of processor uses multiple instructions grouped together. Under software control (normally the compiler) instructions are grouped into blocks of 8 as a single VLIW. These blocks of 8 instructions are dispatched to the multiple functional units of the VLIW pipeline. A single VLIW in C6x terminology is referred to as an Instruction Packet.... [An] Instruction Dispatch/Decode unit 115 decodes these component instructions, schedules them and lastly dispatches them to the specific function unit (S, L, M or D) and sides as indicated by the instruction.

Shiell, Col. 3, line 62 - Col. 4, line 8.

The system in Shiell is described with respect to FIG. 2 as follows:

> Fetch program counter and control units 110A and 110B ***each fetch a half packet of instructions, (1/2 of a VLIW eight instruction packet)*** from program memory 105 (which is now dual ported), into respective Instruction Dispatch/Decode units 115A and 115B.... Then each side's dispatch and decode logic 115A and 115B prepares the half packets for execution as per a "normal" C6x. After which the instructions are dispatched to their respective sides (instructions on A side to the A functional units S1, L1, M1 and D1, and B instructions to the B units S2, L2, M2 and D2). From dispatch on the processor acts as a "normal" C6x except for the handing of changes in control flow such as interrupts and branches.[sic]

Shiell, Col. 4, line 67 - Col. 5, line 13 (*emphasis added*).

For further illustration, Shiell states:

> The following is an example of how a C6x system modified according to this invention converts from running a single thread in single PC mode, as in FIG. 1, to running dual threads in dual PC mode, as in FIG. 2....

Shiell, Col. 6, lines 19-22.

Figures 1 and 2 are provided below to better illustrate the differences between the present invention and the teachings of Shiell. Figure 1 is an example illustration of the present invention. In Figure 1, a VLIW includes multiple instructions (i.e., Instructions 1 and 2). Instruction 1 includes multiple operations (i.e., Operations 1 and 2), and Instruction 2 includes a single operation (i.e., Operation 3). As shown in Figure 1, an instruction of the VLIW may include a single operation or multiple operations.

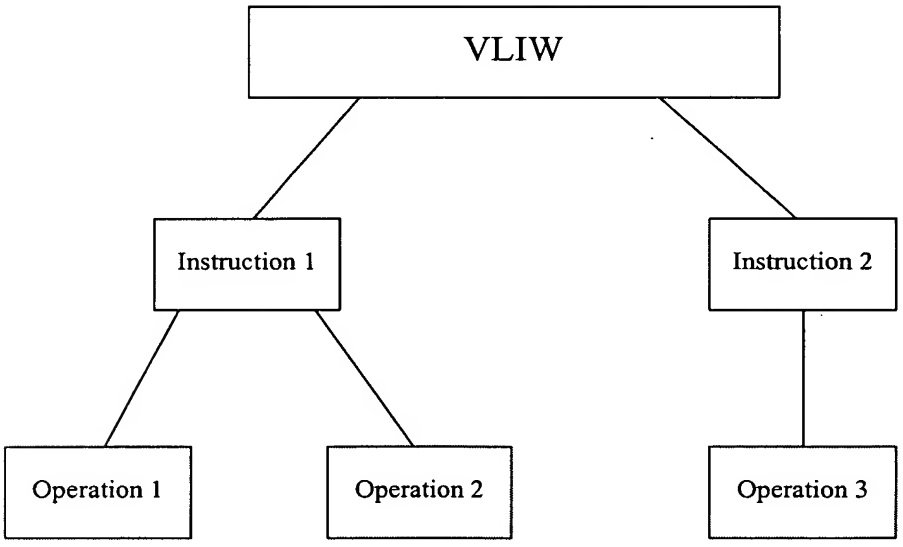

Figure 1

Shiell describes processing a VLIW using a single PC mode and alternatively using a dual PC mode. The single PC mode is described as conventional processing of a VLIW as known in the art. For example, the VLIW is processed as a single stream of instructions. Figure 2 illustrates the dual PC mode described in Shiell. As shown in Figure 2, a VLIW of eight instructions is separated into two half-packets, which are also referred to as streams. Each half-packet/stream includes four instructions. The half-packets may be processed on respective sides of a data processor. Alternatively, instructions may be processed alternately from the half-packets. The processor in Shiell is not described as allowing an instruction of the VLIW to define two independent operations.

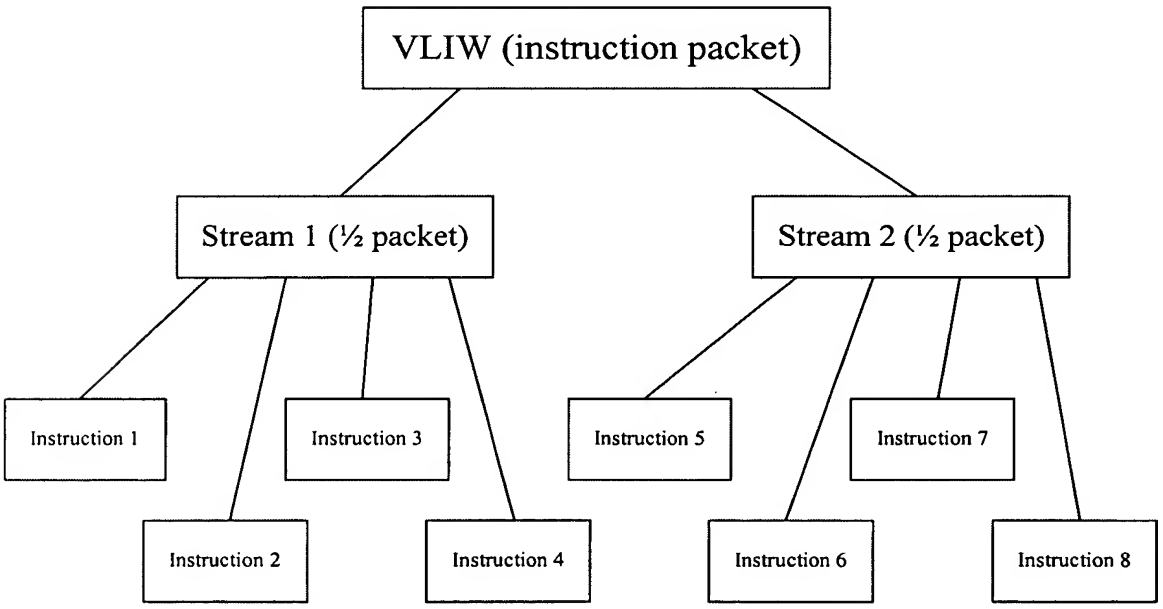

Figure 2

The Examiner contends that Shiell teaches a processor that performs two independent operations. However, the alleged "two independent operations" to which the Examiner refers are each merely a half-packet of instructions (1/2 of a VLIW eight instruction packet). Thus, each of the "two independent operations" is merely a group of four instructions of the VLIW.

Therefore, Shiell does not teach or suggest a decode unit that is operable to determine whether an instruction of a VLIW defines a single operation or two independent operations, as set forth in independent claim 17.

Accordingly, the rejection of claim 17 under 35 U.S.C. § 102(b) is improper and must be reversed.

Claim 18

Claim 18 recites, among other features,

> when ***the decode unit determines that the instruction defines two independent operations***....

In Shiell, a half-packet of instructions is fetched into each of the Instruction Dispatch/Decode units 115A and 115B. "Instruction Adapter units 217A and 217B bind the instructions to the A and B sides respectively. Then each side's dispatch and decode logic 115A and 115B prepares the half packets for execution as per a 'normal' C6x" (Shiell, Col. 4, line 67 - Col. 5, line 8). Thus, Decode units 115 operate the same, regardless whether the VLIW is processed using a single PC mode or a dual PC mode. Nothing in Shiell even suggests that the decode unit determines that the instruction defines two independent operations, as set forth in claim 18.

Accordingly, the rejection of claim 18 under 35 U.S.C. § 102(b) is improper and must be reversed.

Claim 19

Claim 19 recites, among other features,

> when ***the decode unit determines that the instruction defines a single operation***....

In Shiell, Decode units 115 operate the same, regardless whether the VLIW is processed using a single PC mode or a dual PC mode. Nothing in Shiell even suggests that the decode unit determines that the instruction defines a single operation, as set forth in claim 19. Accordingly, the rejection of claim 19 under 35 U.S.C. § 102(b) is improper and must be reversed.

Claim 20

Claim 20 recites, among other features,

> ***the first and second processing channels share at least one common register file and are capable of simultaneously accessing the at least one common register file.***

Shiell merely states that "each instruction on A side 130A or B side 130B has its register arguments read from the associated register file 140A or 140B. In addition, one cross register read is allowed per side via register cross path 145." (Shiell, Col. 4, lines 25-28). Nothing in Shiell even suggests that the first and second processing channels share at least one common register file and are capable of simultaneously accessing the at least one common register file, as set forth in claim 20. Accordingly, the rejection of claim 20 under 35 U.S.C. § 102(b) is improper and must be reversed.

Claim 24

Claim 24 recites, among other features,

> ***decoding an instruction of the VLIW ... to determine whether the instruction defines a single operation or two independent operations***;
>
> when ***the instruction defines two independent operations....***

As described above and further illustrated in Figure 2, Shiell does not teach or suggest decoding an instruction of the VLIW to determine whether the instruction defines a single operation or two independent operations, as set forth in Appellant's claim 24. Moreover, Shiell does not even suggest that the instruction defines two independent operations, as set forth in Appellant's claim 24. Accordingly, the rejection of claim 24 under 35 U.S.C. § 102(b) is improper and must be reversed.

Claim 25

Claim 25 recites, among other features,

> ***determining whether the instruction defines the single operation or the two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction.***

The Office Action merely stated that "claim 25 has nothing over claim 21 and is therefore rejected for the same reasons as set forth in claim 21." However, claim 21 was rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Shiell in view of Yoshida. The Appellant asserts that the rejection of claim 25 under 35 U.S.C. § 102(b) is improper for at least the reason that the rejection is based on a combination of references.

Moreover, at paragraph 11 of the Office Action, the Examiner conceded that "Shiell et al. have not specifically taught wherein the decode unit is operable to determine whether the instruction defines a single operation or two independent

operations based on at least one identification bit at at least one predetermined bit location in the instruction."

Referring to the rejection of claim 21, the Examiner relied on Figure 25 and elements 505 and 506 of Yoshida to allegedly show the teachings missing from Shiell. However, Figure 25 of Yoshida merely shows a VLIW format in which one or two 1-bit format fields are used and one VLIW includes one or two instructions. The confusion appears to be a matter of semantics.

In the present patent application, a VLIW is referred to as a VLIW, and the instructions in the VLIW are referred to as VLIW instructions. For example, the Background to the Invention section of the present patent application provides:

> ... a number of instructions are retrieved from memory in each instruction fetch, each instruction fetch having a certain bit length and each individual instruction (slot) having a certain bit length (so-called VLIW instructions).

However, it appears that in Yoshida, a VLIW is referred to as a VLIW instruction, and the instructions that are included in the VLIW are referred to as operations. For example, Yoshida explains in the Background of the Invention section:

> The present invention relates to a data processor for performing a plurality of operations in parallel at a high efficiency by executing a so-called VLIW ... type instruction which specifies a plurality of operations by one instruction.

Yoshida, Col. 1, lines 9-15. Yoshida further explains:

> [T]he VLIW technique is a parallel operation technique in which ***one instruction consists of a plurality of parallel executable operations***.... A plurality of operations which are specified by this long instruction word are executed in parallel. ***These types of conventional data processors*** ... guarantee[] that instructions have the same length and

> all of a plurality of operations which are described within one instruction can be executed in parallel....

Yoshida, Col. 1, lines 25-48 (emphasis added).

In a conventional VLIW processor, VLIWs have the same length and all of the instructions in the VLIW can be executed in parallel. VLIWs (i.e. "instructions" as described by Yoshida) are retrieved from memory in each instruction fetch. Moreover, in a conventional VLIW processor, instructions are not capable of defining two independent operations. The instructions and operations described by Yoshida correspond to the VLIWs and instructions, respectively, described in the present patent application.

Yoshida does not supply the teachings missing from Shiell. Therefore, Shiell and Yoshida, considered alone or in combination, do not teach or suggest determining whether the instruction defines a single operation or two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction, as set forth in Appellant's claim 25. Accordingly, claim 25 is patentable over Shiell and Yoshida, considered alone or in any rational combination.

For at least the reasons set forth above, the rejection of claim 25 under 35 U.S.C. § 102(b) is improper and must be reversed.

B. The rejection of claims 21-23, 26, 27, and 32 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Shiell in view of Yoshida is improper and must be reversed

In section 5 of the final Office Action, the Examiner rejected claims 21-23, 26, 27, and 32 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Shiell in

view of Yoshida. Appellant respectfully traverses this rejection. The patentability of each of claims 21-23, 26, 27, and 32 is separately discussed below.

Claim 21

Claim 21 recites, among other features,

> the decode unit is operable to ***determine whether the instruction defines a single operation or two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction***.

The Final Rejection incorporated by reference the several grounds of rejection set forth in the Office Action. At paragraph 11 of the Office Action, the Examiner conceded that "Shiell et al. have not specifically taught wherein the decode unit is operable to determine whether the instruction defines a single operation or two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction." The Examiner relied on Figure 25 and elements 505 and 506 of Yoshida to allegedly show the teachings missing from Shiell. However, Figure 25 of Yoshida merely shows a VLIW format in which one or two 1-bit format fields are used and one VLIW includes one or two instructions. In Yoshida, each 1-bit format field corresponds to a respective instruction. For example, in Figure 25 of Yoshida, VLIW 501 includes format fields 505 and 506 corresponding to respective instructions 511 and 512, and VLIW 502 includes format field 505 corresponding to instruction 513. As shown in Figure 25 of Yoshida, a VLIW that includes one format field includes one instruction, and a VLIW that includes two format fields includes two instructions. Nothing in Yoshida even suggests that a decode unit is operable to determine whether an instruction of a VLIW defines a

single operation or two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction, as set forth in Appellant's claim 21. Thus, Yoshida fails to supply the teachings missing from Shiell.

Therefore, Shiell and Yoshida, considered alone or in any rational combination, do not teach or suggest that a decode unit is operable to determine whether an instruction of a VLIW defines a single operation or two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction, as set forth in Appellant's claim 21.

Accordingly, the rejection of claim 21 under 35 U.S.C. § 103(a) is improper and must be reversed.

Claim 22

Claim 22 recites, among other features,

> the instruction has a length of n bits, and ***the at least one predetermined bit location includes the n/2th bit and the nth bit.***

The Examiner relies on elements 505 and 506 in Figure 25 of Yoshida to allegedly teach the nth and n/2th bits, respectively, of the instruction in Appellant's claim 22. However, upon closer inspection, elements 505 and 506 are not at predetermined bit locations ***in an instruction*** of the VLIW. Instead, element 505 corresponds to instruction 511 of VLIW 501, and element 506 corresponds to instruction 512 of VLIW 501. Elements 505 and 506 do not correspond to the nth and n/2th bits, respectively, of an instruction (or even the VLIW 501). Bits of the VLIW 501 are clearly numbered from 0 to 31, such that n=32. Because the bits of the VLIW are numbered from 0 to 31, the bit labeled "0" is the first bit of the VLIW, the bit

labeled "1" is the second bit, and so on. Thus, element 505 in Figure 25 corresponds to the first bit of VLIW 501, and element 506 corresponds to the seventeenth, (n/2+1)th, bit of the VLIW 501.

Shiell and Yoshida, considered alone or in combination, do not teach or suggest that the at least one predetermined bit location includes the n/2th bit and the nth bit, as set forth in Appellant's claim 22. Therefore, the Examiner has not met the burden required to maintain a *prima facie* case of obviousness with respect to claim 22 for at least the reason that the cited references do not teach each and every feature of Appellant's claim 22.

Accordingly, the rejection of claim 22 under 35 U.S.C. § 103(a) is improper and must be reversed.

Claim 23

Claim 23 recites, among other features,

> the ***decode unit is operable to identify certain combinations of the two independent operations based on the at least one identification bit, and wherein a first combination denotes two data processing operations, a second combination denotes two memory access operations, a third combination denotes a data processing operation and a memory access operation, and a fourth combination denotes a long instruction***.

The Examiner relies on Col. 2, lines 23-56 and Col. 3, line 50 - Col. 4, line 9 of Shiell to allegedly teach the feature of claim 23 recited above. However, the Examiner merely states that the first three combinations are identified when an instruction from side A and an instruction from side B are dispatched to certain of the S, L, M, or D functional units, and the fourth combination denotes a long instruction. Nothing in the cited material or in Yoshida even suggests a decode unit that is

operable to identify certain combinations of the two independent operations [of an instruction of a VLIW] ***based on the at least one identification bit*** [at at least one predetermined location in the instruction], as set forth in Appellant's claim 23.

The Examiner has not met the burden required to maintain a *prima facie* case of obviousness with respect to claim 23 for at least the reason that the cited references do not teach each and every feature of Appellant's claim 23. Accordingly, the rejection of claim 23 under 35 U.S.C. § 103(a) is improper and must be reversed.

Claim 26

Claim 26 recites, among other features,

> ***determining whether the instruction defines the single operation or the two independent operations based on the at least one identification bit that indicates the nature of the two independent operations when the instruction defines the two independent operations.***

At paragraph 14 of the Office Action, the Examiner merely stated that "claim 26 has nothing over claim 21 and is therefore rejected for the same reasons as set forth in claim 21." It is Appellant's position that claim 26 is patentable over Shiell and Yoshida, considered alone or in combination, for at least the same reasons as those set forth above with respect to claim 21. Moreover, nothing in the combination of Shiell and Yoshida teaches or suggests determining whether the instruction defines the single operation or the two independent operations based on the at least one identification bit that indicates the nature of the two independent operations when the instruction defines the two independent operations, as set forth in Appellant's claim 26.

The Examiner has not met the burden required to maintain a *prima facie* case of obviousness with respect to claim 26 for at least the reason that the cited references do not teach each and every feature of Appellant's claim 26. Accordingly, the rejection of claim 26 under 35 U.S.C. § 103(a) is improper and must be reversed.

Claim 27

Claim 27 recites, among other features,

> ***determining whether the instruction defines the single operation or the two independent operations is based on an n/2th bit and an nth bit of the instruction having n bits.***

At paragraph 15 of the Office Action, the Examiner merely stated that "claim 27 has nothing over claim 6 and are [sic] therefore rejected for the same reasons as set forth in claim 6." Claim 6 is cancelled. Nevertheless, Shiell or Yoshida, considered alone or in combination, do not teach or suggest that determining whether the instruction defines the single operation or the two independent operations is based on an n/2th bit and an nth bit of the instruction having n bits, as set forth in Appellant's claim 27. For example, in Figure 25 of Yoshida, elements 505 and 506 do not correspond to the nth and n/2th bits, respectively, of an instruction (or even the VLIW 501). Instead, element 505 in Figure 25 corresponds to the first bit of VLIW 501, and element 506 corresponds to the seventeenth, (n/2+1)th, bit of the VLIW 501.

The Examiner has not met the burden required to maintain a *prima facie* case of obviousness with respect to claim 27 for at least the reason that the cited references do not teach each and every feature of Appellant's claim 27. Accordingly, the rejection of claim 27 under 35 U.S.C. § 103(a) is improper and must be reversed.

Claim 32

Claim 32 recites, among other features,

> decoding each instruction of the VLIW, wherein decoding each instruction includes ***reading the identification bit of each instruction to determine ... whether the instruction defines a single operation or two independent operations***...

In paragraph 12 of the Final Rejection, the Examiner conceded that Shiell fails to teach decoding that includes reading the identification bit of each instruction to determine whether the instruction defines a single operation or two independent operations. The Examiner relied on Figure 25 and elements 505 and 506 of Yoshida to allegedly show the missing teachings. However, Figure 25 of Yoshida merely shows a VLIW format in which one or two 1-bit format fields are used and one VLIW includes one or two instructions. Shiell and Yoshida, considered alone or in combination, do not teach or suggest reading the identification bit of each instruction to determine whether the instruction defines a single operation or two independent operations, as set forth in Appellant's claim 32.

The Examiner has not met the burden required to maintain a *prima facie* case of obviousness with respect to claim 32 for at least the reason that the cited references do not teach each and every feature of Appellant's claim 32. Accordingly, the rejection of claim 32 under 35 U.S.C. § 103(a) is improper and must be reversed.

C. The rejection of claim 28 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Shiell in view of Panesar is improper and must be reversed

In section 6 of the final Office Action, the Examiner rejected claim 28 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Shiell in view of Panesar. Appellant respectfully traverses this rejection.

Claim 28

Claim 28 recites, among other features,

> ...commands to enable the processor-based system to ***decode an instruction of the VLIW*** received during an instruction fetch ***to determine whether the instruction defines a single operation or two independent operations***...

Appellant asserts that Shiell does not teach or suggest *commands to enable the processor-based system to decode an instruction of the VLIW ... to determine whether the instruction defines a single operation or two independent operations*, as set forth in Appellant's claim 28.

Appellant further asserts that Panesar has nothing to do with determining whether an instruction of a VLIW defines a single operation or two independent operations.

In paragraph 13 of the Final Rejection, the Examiner stated:

> [T]he fact that Panesar may have nothing to do with "determining whether an instruction of a VLIW defines a single operation or two independent operations" is irrelevant because Panesar has been cited for teaching the simulation of a processor with commands such as VHDL (Panesar, column 8, lines 25-36).

Final Rejection, dated October 19, 2004, at p. 5.

Nevertheless, Panesar does not supply the teachings missing from Shiell. Thus, Shiell and Panesar, considered alone or in combination, do not teach or suggest *commands to enable the processor-based system to decode an instruction of the VLIW ... to determine whether the instruction defines a single operation or two independent operations*, as set forth in Appellant's claim 28.

The Examiner has not met the burden required to maintain a *prima facie* case of obviousness with respect to claim 28 for at least the reason that the cited references do not teach each and every feature of claim 28. Accordingly, the rejection of claim 28 under 35 U.S.C. § 103(a) is improper and must be reversed.

D. The rejection of claims 29-31 and 33 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Shiell in view of Yoshida and Panesar is improper and must be reversed

In section 7 of the final Office Action, the Examiner rejected claims 29-31 and 33 under 35 U.S.C. § 103(a) as being allegedly unpatentable over Shiell in view of Yoshida and Panesar. Appellant respectfully traverses this rejection. The patentability of each of claims 29-31 and 33 is separately discussed below.

Claim 29

Claim 29 recites, among other features,

> ...commands to enable the processor-based system to ***decode the instruction*** [of the VLIW] ***to determine whether the instruction defines the single operation or the two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction***.

In the Office Action, the Examiner conceded that the combination of Shiell and Panesar does not teach commands to enable the processor-based system to decode

the instruction [of the VLIW] to determine whether the instruction defines the single operation or the two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction. The Examiner relied on elements 505 and 506 in Figure 25 of Yoshida to allegedly show the teachings missing from Shiell and Panesar. However, Figure 25 of Yoshida merely shows a VLIW format in which one or two 1-bit format fields are used and one VLIW includes one or two instructions. In Yoshida, each 1-bit format field corresponds to a respective instruction. For example, in Figure 25 of Yoshida, VLIW 501 includes format fields 505 and 506 corresponding to respective instructions 511 and 512, and VLIW 502 includes format field 505 corresponding to instruction 513. As shown Figure 25 of Yoshida, a VLIW that includes one format field includes one instruction, and a VLIW that includes two format fields includes two instructions. Nothing in Yoshida even suggests commands to enable the processor-based system to decode the instruction [of the VLIW] to determine whether the instruction defines the single operation or the two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction, as set forth in Appellant's claim 29. Thus, Yoshida fails to supply the teachings missing from Shiell and Panesar.

Therefore, Shiell, Yoshida, and Panesar, considered alone or in any rational combination, do not teach or suggest commands to enable the processor-based system to decode the instruction [of the VLIW] to determine whether the instruction defines the single operation or the two independent operations based on at least one

identification bit at at least one predetermined bit location in the instruction, as set forth in Appellant's claim 29.

Accordingly, the rejection of claim 29 under 35 U.S.C. § 103(a) is improper and must be reversed.

Claim 30

Claim 30 recites, among other features,

> ...commands to enable the processor-based system to ***decode the instruction*** [of the VLIW] ***to determine whether the instruction defines the single operation or the two independent operations based on the at least one identification bit that indicates the nature of the two independent operations when the instruction defines the two independent operations***.

The Examiner relied on elements 505 and 506 in Figure 25 of Yoshida to allegedly show the feature of claim 30 recited above. However, elements 505 and 506 correspond to separate instructions of a VLIW, and therefore do not indicate the nature of two independent operations when an instruction defines the two independent operations, as set forth in Appellant's claim 30.

Shiell, Yoshida, and Panesar, considered alone or in combination, do not teach each and every feature of Appellant's claim 30. Therefore, the Examiner has not met the burden required to maintain a *prima facie* case of obviousness with respect to claim 30.

Accordingly, the rejection of claim 30 under 35 U.S.C. § 103(a) is improper and must be reversed.

Claim 31

Claim 31 recites, among other features,

> ...commands to enable the processor-based system to ***decode the instruction*** [of the VLIW] ***to determine whether the instruction defines the single operation or the two independent operations based on an n/2th bit and an nth bit of the instruction having n bits.***

The Examiner relies on elements 505 and 506 in Figure 25 of Yoshida to allegedly teach the nth and n/2th bits, respectively, of the instruction in Appellant's claim 31. However, element 505 corresponds to instruction 511 of the VLIW, and element 506 corresponds to instruction 512 of VLIW 501. Furthermore, elements 505 and 506 do not correspond to the nth and n/2th bits, respectively, of an instruction (or even the VLIW 501).

Shiell, Yoshida, and Panesar, considered alone or in combination, do not teach or suggest commands to enable the processor-based system to decode the instruction [of the VLIW] to determine whether the instruction defines the single operation or the two independent operations based on an n/2th bit and an nth bit of the instruction having n bits, as set forth in Appellant's claim 31.

The Examiner has not met the burden required to maintain a *prima facie* case of obviousness with respect to claim 31 for at least the reason that the cited references do not teach each and every feature of Appellant's claim 31. Accordingly, the rejection of claim 31 under 35 U.S.C. § 103(a) is improper and must be reversed.

Claim 33

Claim 33 recites, among other features,

> ...commands to enable the processor-based system to ***decode an instruction of the VLIW*** received during an instruction fetch ***to***

determine ... whether the instruction defines a single operation or two independent operations...

In the Office Action, the Examiner merely stated that "claim 33 has nothing over claims 17-31 and is therefore rejected for the same reasons as set forth in claims 17-31." Thus, claim 33 is patentable over Shiell, Yoshida, and Panesar, considered alone or in combination, for at least the same reasons as those set forth above with respect to claims 17-31. Moreover, nothing in the combination of Shiell, Yoshida, and Panesar teaches or suggests commands to enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch to determine ... whether the instruction defines a single operation or two independent operations, as set forth in Appellant's claim 33.

The Examiner has not met the burden required to maintain a *prima facie* case of obviousness with respect to claim 33 for at least the reason that the cited references do not teach each and every feature of Appellant's claim 33. Accordingly, the rejection of claim 33 under 35 U.S.C. § 103(a) is improper and must be reversed.

VIII. Conclusion

The subject matter of claims 17-33 is patentable over the cited art because the Examiner has failed to show that each and every feature of the claimed embodiments is taught in the cited references. Therefore, Appellant respectfully requests that the Board reverse the Examiner's final rejection of these claims under 35 U.S.C. §§ 102(b) and 103(a) and remand this application for allowance and issue.

Respectfully submitted,

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Claims Appendix

17. A system to process very long instruction words (VLIWs), the system comprising:

a decode unit to decode an instruction of a VLIW received during an instruction fetch, wherein all instructions of the VLIW have the same predetermined instruction bit length; and

first and second processing channels, each processing channel including a plurality of functional units, at least one of the functional units of each processing channel being a data processing unit and at least one other of the functional units of each processing channel being a memory access unit;

wherein the decode unit is operable to determine whether the instruction defines a single operation or two independent operations and to control the first and second processing channels based on the determination.

18. The system according to claim 17, wherein, when the decode unit determines that the instruction defines two independent operations, the decode unit is operable to control the first channel to implement one of the two independent operations and the second channel to implement the other of the two independent operations, and wherein the first and second channels execute their respective independent operations simultaneously.

19. The system according to claim 17, wherein, when the decode unit determines that the instruction defines a single operation, the decode unit is operable to control the first and second processing channels to cooperate to execute the single operation.

20. The system according to claim 17, wherein the first and second processing channels share at least one common register file and are capable of simultaneously accessing the at least one common register file.

21. The system according to claim 17, wherein the decode unit is operable to determine whether the instruction defines a single operation or two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction.

22. The system according to claim 21, wherein the instruction has a length of n bits, and the at least one predetermined bit location includes the n/2th bit and the nth bit.

23. The system according to claim 21, wherein the decode unit is operable to identify certain combinations of the two independent operations based on the at least one identification bit, and wherein a first combination denotes two data processing operations, a second combination denotes two memory access operations, a third combination denotes a data processing operation and a memory access operation, and a fourth combination denotes a long instruction.

24. A method of operating a system that processes very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length, the method comprising:

decoding an instruction of the VLIW received during an instruction fetch to determine whether the instruction defines a single operation or two independent operations;

when the instruction defines two independent operations, supplying one of the independent operations to a first processing channel having a first plurality of functional units including a first data processing unit and a first memory access unit, and supplying the other of the independent operations to a second processing channel having a second plurality of functional units including a second data processing unit and a second memory access unit, wherein the two independent operations are executed simultaneously; and

when the instruction defines a single operation, controlling the first and second processing channels to cooperate to execute the single operation.

25. The method according to claim 24, wherein decoding the instruction includes determining whether the instruction defines the single operation or the two independent

operations based on at least one identification bit at at least one predetermined bit location in the instruction.

26. The method according to claim 25, wherein determining whether the instruction defines the single operation or the two independent operations includes determining whether the instruction defines the single operation or the two independent operations based on the at least one identification bit that indicates the nature of the two independent operations when the instruction defines the two independent operations.

27. The method according to claim 25, wherein determining whether the instruction defines the single operation or the two independent operations is based on an n/2th bit and an nth bit of the instruction having n bits.

28. An article comprising a medium for storing commands to enable a processor-based system to:

process very long instruction word data including very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length, wherein the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch to determine whether the instruction defines a single operation or two independent operations;

when the instruction defines two independent operations, supply one of the independent operations to a first processing channel and supply the other of the independent operations to a second processing channel, wherein the two independent operations are executed simultaneously; and

when the instruction defines a single operation, control the first and second processing channels to cooperate to execute the single operation.

29. The article according to claim 28, wherein the commands to enable the processor-based system to decode the instruction include the commands to enable the processor-based

system to decode the instruction to determine whether the instruction defines the single operation or the two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction.

30. The article according to claim 29, wherein the commands to enable the processor-based system to decode the instruction include the commands to enable the processor-based system to decode the instruction to determine whether the instruction defines the single operation or the two independent operations based on the at least one identification bit that indicates the nature of the two independent operations when the instruction defines the two independent operations.

31. The article according to claim 29, wherein the commands to enable the processor-based system to decode the instruction include the commands to enable the processor-based system to decode the instruction to determine whether the instruction defines the single operation or the two independent operations based on an n/2th bit and an nth bit of the instruction having n bits.

32. A method of operating a system that processes very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length and at least one identification bit at at least one predetermined bit location in the instruction, the method comprising:

fetching the VLIW from a program memory;

decoding each instruction of the VLIW, wherein decoding each instruction includes reading the identification bit of each instruction to determine:

a) whether the instruction defines a single operation or two independent operations, and

b) when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation.

33. An article comprising a medium for storing commands to enable a processor-based system to:

process very long instruction word data including very long instruction words (VLIWs), each instruction of a VLIW having the same predetermined instruction bit length and at least one identification bit at at least one predetermined bit location in the instruction, wherein the commands to enable the processor-based system to process the very long instruction word data include commands to enable the processor-based system to decode an instruction of the VLIW received during an instruction fetch to determine:

a) whether the instruction defines a single operation or two independent operations, and

b) when the instruction defines two independent operations, the nature of each of the two independent operations selected at least from a data processing category of operation and a memory access category of operation.

Evidence Appendix

To the best of the knowledge of Appellant, Appellant's legal representative, and Appellant's assignee, there has been no evidence submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132, nor has any other evidence been entered in the record by the Examiner and relied upon in this Appeal Brief.

Related Proceedings Appendix

To the best of the knowledge of Appellant, Appellant's legal representative, and Appellant's assignee, there are no other appeals or interferences which will directly affect or be directly affected or have a bearing on a decision by the Board of Patent Appeals and Interferences ("the Board") in the pending appeal.